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RIPPLE CARRY ADDERS USING LOW-VOLTAGE BOOSTED CMOS DRIVERS

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ABSTRACT

This paper describes a high speed boosted CMOS differential logic which is used in ripple carry adders. The proposed logic style improves switching speed by boosting the gate–source voltage of transistors along timing-critical signal paths. Test sets of logic gates were designed in a 0.18-µm CMOS process, whose comparison results indicated that the energy–delay product of the proposed logic style was improved by up to 50% compared with conventional logic styles at supply voltage of 1.8V. The experimental result for 32 bit ripple carry adder using the proposed logic style revealed that the addition time is reduced as compared with the conventional CMOS circuits.

Keywords- *Adder, Low Power, Low Voltage, Voltage Boosting, Addition Time*.

INTRODUCTION

Bootstrapping is an effective method for speed improvement and power reduction. One of the famous methods to decrease the power consumed by a CMOS digital circuit is scaling of supply voltage.This is due to the fact that the switching power consumed by the circuit has a quadratic relationship with supply voltage. In certain cases, the circuit is made in a way to operate in the sub threshold region for achieving maximum energy efficiency. However this idea is restricted and used in a design of low end where speed is taken as the secondary concern due to severe speed degradation because of small switch current and variability of high performance due to the variations in process, temperature and threshold voltage. For designing a medium and high end in which performance of the speed and energy efficiency both gets importance, no acceptance of large aggressive scaling of voltage and then a close threshold voltage design is more accurate for gaining relatively high energy efficiency in the absence of severe speed degradation. The method of voltage scaling helps in reducing the total power consumption of a system. In applications where high speed is necessary differential cascade voltage switch is neglected due to the insufficient speed of the circuit. Furthermore, domino logic is not suitable due to the reduction of overdrive voltage. As the scaling of supply voltage approaches the threshold voltage the performance of the speed of previous CMOS circuits like logic of static CMOS, logic of the differential cascade voltage switch (DCVS) [see Fig. 1(a)] and logic of the domino CMOS [see Fig. 1(b)] is degraded due to the reduction in overdrive voltage (VGS – VTH) of transistors. To eliminate this problem, a bootstrapped CMOS containing large capacitive load driver was suggested. It was a solution to problem of speed degradation. It can enhance the switching speed at supply voltage which is low by giving the voltage of some inherent nodes goes boosted beyond the supply rails. In this two capacitors are utilize for the purpose of bootstrapping. However this circuit was suggested for used as a driver of large capacitive load, logic fuctions cannot be effectively fit into the circuit and the benefits of speed was not completely exploited. For the operation of fast logic with low supply voltage, BDL known as CMOS bootstrapped dynamic logic was suggested [see Fig.1(c)]. However, the speed of this BDL was not improved too much due to the latent bulky bootstrapped circuit which was superimposed over the entire latency of the circuit. Moreover, there is a restriction of composition of logic of this BDL since it is referred as a one ended structure.

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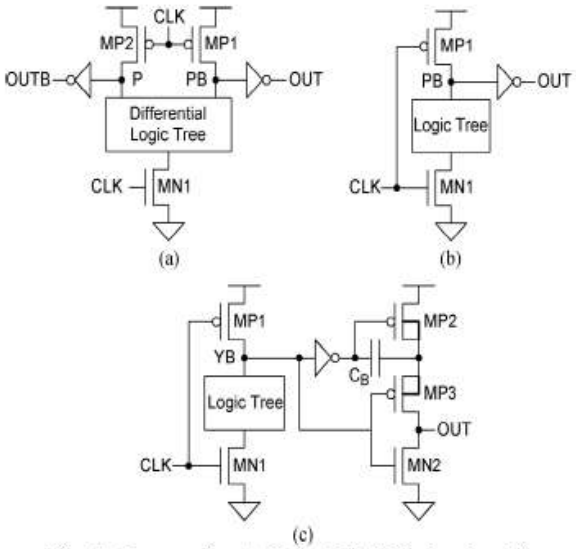

Fig. 1. Conventional digital CMOS circuits. (a) DCVS. (b) Domino CMOS logic. (c) BDL.

To overcome the above problem BCDL differential logic style was suggested. It is not only better in terms of improving switching speed but also reduces area due to sharing of single boosting circuit. Switching speed is better due to the boosting of overdrive voltage along the path of critical timing signal. Furthermore the problem of latency can be removed by allowing the block of voltage boosting directly to the tree of differential logic.

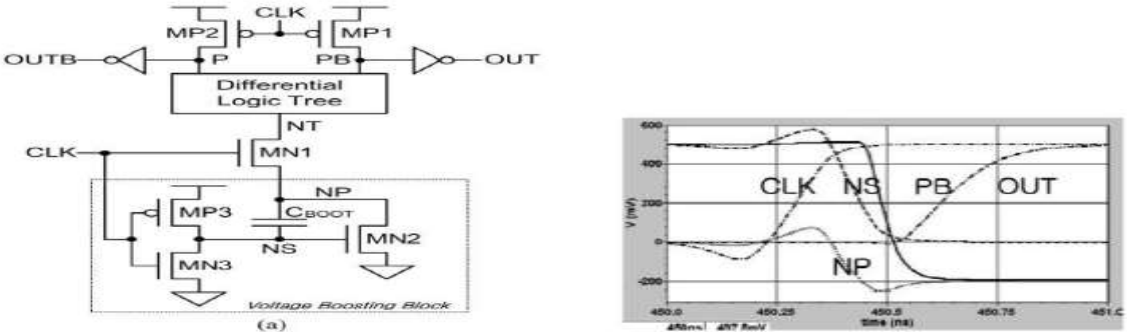

Fig. 2 (a) BCDL structure (b) Simulated waveforms

It contains a differential logic block referred as precharged and a voltage boosting block. The lower part of the circuit is known as voltage-boosting block, which is given in the dotted box consists of transistors known as MN2, MN3, and MP3 and CBOOT referred as boosting capacitor and is utilized in boosting of the voltage of NP approaches below the ground. The logic block known as precharged differential, which is made of a tree of differential logic with bottom transistor namely MN1, precharge transistors known as MP1 and MP2 and output inverters receives the boosted voltage at NP and evaluates the value of the output logic. Its operation is taking place in two phases known as a precharge phase and a phase of boosted evaluation. The circuit follows precharge phase when the value of CLK is low. During precharge phase, separation of the precharge differential logic block from the block of voltage boosting takes placed due to the turn of MN1. Precharge nodes known as P and PB that are in the differential logic block are precharged to the supply voltage with the help of MP1 and MP2 resulting in outputs namely OUT and OUTB low. During the similar time, turn on of the transistors referred as MP3 and MN2 in the block of voltage boosting takes place resulting NS to be high and NP to be low. Then a voltage that is similar to the supply voltage is applied to CBOOT. When CLK changes from low to high then the circuit comes into the boosted evaluation phase. The executed waveforms in this phase of BCDL are shown in Fig. in which utilization of supply voltage of 0.5V is used. When CLK rises to high then turn on of MN1 takes place and connection of the differential logic tree to the block of voltage boosting block is operated. During this time pull down of NS takes place toward the ground result in boosting of NP

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and NT below the ground with the help of capacitive coupling carried through CBOOT. As given in Fig. , NP temporary reach at -250 mV and settles at near -200 mV by the action of boosting. Then the MN1 gate to source voltage and transistors that are in the logic in driving strength of all these transistors. However, a little forward in the voltage of source body established in these transistors using boosting source voltages approaches below the ground leads resulting a decrease in threshold voltage of all these transistors, further increase their driving strength. Meanwhile, the boosted voltage appearing at NT is then goes to P or PB is pulled down below the ground. Then, there is an enlargement in the gate source voltage of the driver PMOS transistor increases its driving strength. Effects of all these driving strength carried out by boosting are then combined together along the path of timing critical signal taken from input to output through nodes of precharging that results in improvement of switching speed at a region of low voltage. Thus it helps in improving switching speed and regarded as a better differential logic style that is used in high speed applications.

SIMULATION COMPARISION

Ripple carry chain of 8 bit was utilizes in the BCDL adder to boost the operation of each carry chain stage whereas a carry chain of 8 bit Manchester was utilized in the adder of DCVS and BDL for propagation of carry of high speed. Fig.3 shows the conventional structure of 8 bit ripple carry chain used in the BCDL adder.

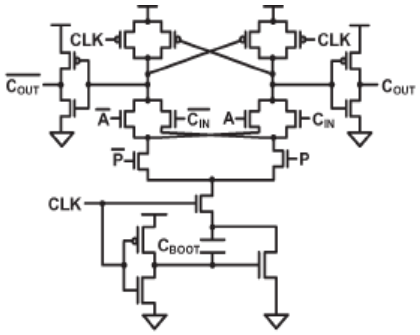

Fig.3. Conventional structure of 8 bit ripple carry chain used in BCDL

XOR GATE

Carry is propagated with the help of XOR gate when both inputs are 1 whereas its generated when either of its input are 1.Fig.4 shows the structure of xor gate for carry propagation.

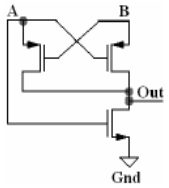

Fig. 4. XOR gate

$P_i = A_i \text{ xor } B_i$ (1)

Table 1 shows the total delay, power consumption and power delay product of proposed 1 bit ripple carry adder as compared with conventional 1 bit ripple carry adder.

Ripple Carry Adder	Rising delay (*)	Falling Delay (*)	Total delay(*)	Power consumption(*)	PDP (&)
22T (Prop.)	.39	.088	19.54	16	313
24T	.39	.22	19.61	16	314
Units- *=ns, &=ns x ns					

Table 1- 1 bit ripple carry adder

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Fig.5 shows the rising delay, propagation delay, power consumption and power delay roduct chart of 1 bit ripple carry adder.

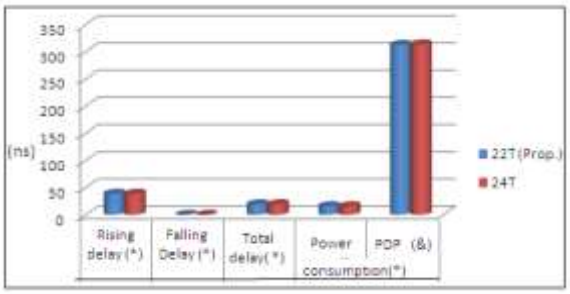

Fig. 5. Rising delay, propagation delay, power consumption and PDP chart of 1 bit ripple carry adder.

EXPERIMENT RESULTS

The experimental result for 32 bit ripple carry adder using the proposed logic style is carried out. In 32 bit adder an 8 bit ripple carry chain is used to allow boosting operation at each carry chain stage. Fig. 6 shows the proposed 8 bit ripple carry chain in BCDL.

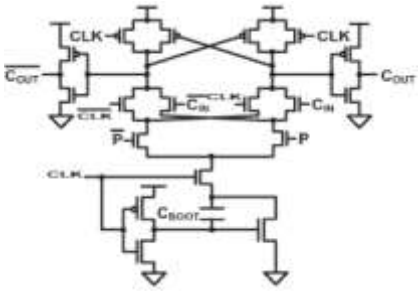

Fig.6. Proposed 8 bit ripple carry chain in BCDL

The proposed structure of 1 bit ripple carry chain in 32 bit BCDL adder is shown in Fig.7

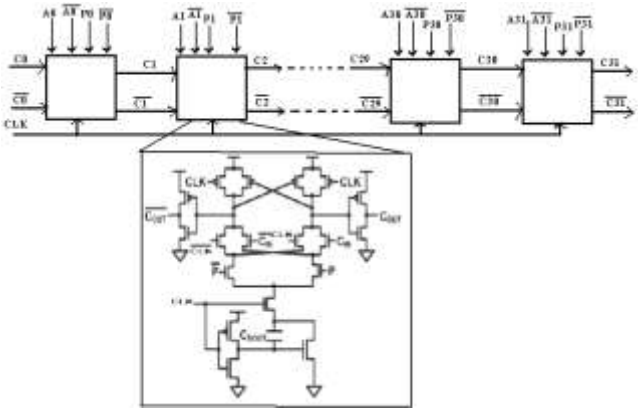

Fig. 7 . structure of 1 bit ripple carry chain in 32 bit BCDL adder

Table 2 shows the total delay,power consumption and power delay product of 32 bit ripple carry adder.

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32 bit Ripple Carry Adder	Rising delay (*)	Falling Delay (*)	Total delay(*)	Power consumption($)	PDP (&)
704T (Prop.)	-39	.14	19.57	10	195
768T	-39	.22	19.61	10	196
Units- *=ns, &=ns x ns $=µm					

Table. 2 . 32 bit ripple carry adder

The rising delay, propagation delay, power consumption and PDP chart of 32 bit ripple carry adder is shown in Fig.8

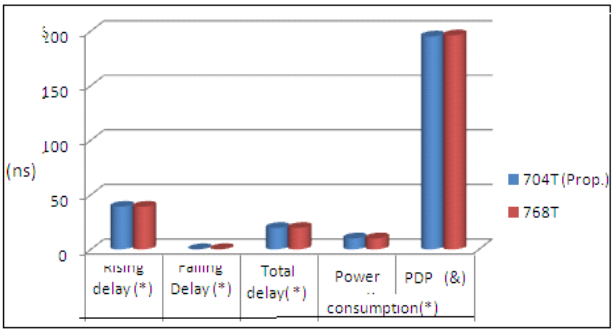

Fig.8 Rising delay, propagation delay, power consumption and PDP chart of 32 bit ripple carry adder

The proposed 8 bit ripple carry adder waveform is shown in Fig. 9

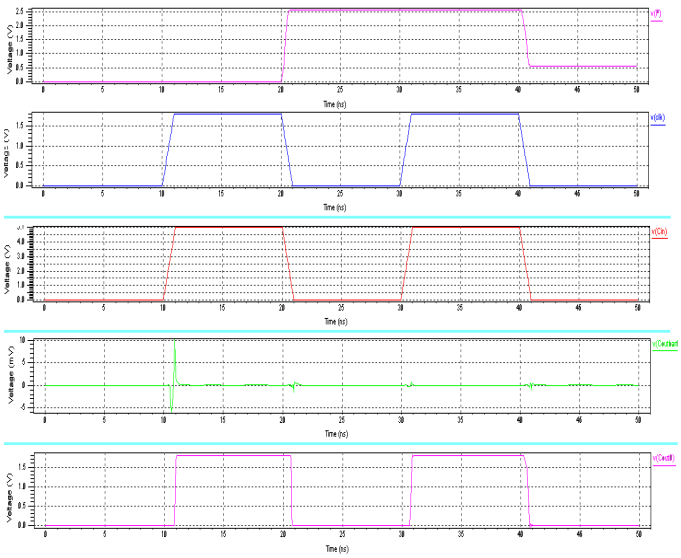

Fig. 9 Proposed 8 bit ripple carry adder waveform

CONCLUSION

CMOS differential logic style with feature of voltage boosting has been described. The BCDL gives better switching speed when compared to conventional logic style at low supply voltage by using a single boosing circuit that is shared by complementary outputs. The BCDL also reduces the area. Comparision results in a tsmc 0.180 um cmos process shows that the energy delay product of the recommended logic style was improved when compared with the conventional logic styles. The experiment result for a 32 bit ripple carry adder using BCDL logic style indicated a reduction in the addition time.

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